

CLAIMS

I claim:

- 5 1. A method for application specific integrated circuit prototyping comprising:
 placing a first block of said application specific integrated circuit in a first programmable logic device wherein said first block
10 generates a plurality of parallel output signals;
 placing a second block of said application specific integrated circuit in a second programmable logic device;
 using a first serial COM wrapper, in said
15 first programmable logic device, to convert said plurality of parallel output signals to a serial data stream; and
 using a second serial COM wrapper, in said
20 second programmable logic device, to convert said serial data stream to said plurality of parallel output signals.
2. The method of Claim 1 further comprising:
 using a plurality of n serializer units in
25 said first COM wrapper, wherein each serializer unit in said plurality of n serializer units processes a different set of output signals in said plurality of parallel output signals to create a serial data stream so that a plurality of
30 n serial data streams are created.
3. The method of Claim 2 further comprising:
 using a plurality of n deserializer units in
35 said second COM wrapper, wherein each deserializer unit in said plurality of n deserializer units

processes a different serial data stream in said plurality of n serial data streams.

4. The method of Claim 1 wherein said first
5 programmable logic device is a field programmable gate array, and said second programmable logic device is another field programmable gate array.

5. A method comprising:
10 processing, in a first programmable logic device containing a block of an application specific integrated circuit being prototyped, a plurality of output signals using a serial COM wrapper to generate at least one serial data
15 stream; and
passing said at least one serial data stream over a serial link to a second serial COM wrapper in a second programmable logic device containing another block of said application specific
20 integrated circuit being prototyped.

6. A structure comprising:
a printed circuit board;
a first programmable logic device, coupled to
25 said printed circuit board, comprising:
a pin; a
a block of an application specific integrated circuit being prototyped wherein said block generates a plurality of output
30 signals; and
a serial COM wrapper coupled to said block to receive a plurality of parallel output signals, and coupled to said pin;
a second programmable logic device, coupled
35 to said printed circuit board, comprising:
another pin;

another block of said application
specific integrated circuit being prototyped;
and

5 another serial COM wrapper coupled to
said another block to provide a plurality of
parallel input signals, and coupled to said
another pin; and
a trace on said printed circuit board
coupling said pin to said another pin.

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7. The structure of Claim 6 wherein said serial
COM wrapper comprises:
at least one serializer unit.

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8. The structure of Claim 6 wherein said serial
COM wrapper comprises:
a plurality of serializer units wherein each
serializer unit is coupled to receive a different
set of output signals in said plurality of output
20 signals.

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9. The structure of Claim 6 wherein said another
serial COM wrapper comprises:
at least one deserializer unit.

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10. The structure of Claim 6 wherein said another
serial COM wrapper comprises:
a plurality of deserializer units wherein
each deserializer unit is coupled to receive a
different serial data stream.
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11. The structure of Claim 6 wherein said first
programmable logic device is a field programmable gate
array, and said second programmable logic device is
35 another field programmable gate array.

12. A structure comprising:
a programmable logic device comprising:
a pin; a
a block of an application specific
5 integrated circuit being prototyped wherein
said block generates a plurality of output
signals; and
a serial COM wrapper coupled to said
block to receive said plurality of parallel
10 output signals, and coupled to said pin.
13. The structure of Claim 12 wherein said serial
COM wrapper comprises:
a serializer coupled to receive said
15 plurality of parallel output signals, and coupled
to said pin.
14. The structure of Claim 13 wherein said
serializer comprises:
20 at least one serializer unit.
15. The structure of Claim 13 wherein said
serializer comprises:
a plurality of serializer units wherein each
25 serializer unit is coupled to receive a different
set of output signals in said plurality of output
signals.
16. The structure of Claim 12 wherein said serial
30 COM wrapper is coupled to said block to provide a
plurality of parallel input signals and said structure
further comprises:
another pin coupled to said serial COM
35 wrapper.

17. The structure of Claim 16 wherein said serial
COM wrapper comprises:

5 a deserializer coupled to said block to
provide said plurality of parallel input signals,
and coupled to said another pin.

18. The structure of Claim 17 wherein said
deserializer comprises:

10 at least one deserializer unit.

19. The structure of Claim 17 wherein said
deserializer comprises:

15 a plurality of deserializer units wherein
each deserializer unit is coupled to provide to
said block a different set of input signals in
said plurality of input signals.

20. The structure of Claim 12 wherein said
programmable logic device is a field programmable gate
20 array.